DESCRIPTION

A CONSTANT-VOLTAGE CIRCUIT

5   TECHNICAL FIELD

         The present invention generally relates to

a constant-voltage circuit, and especially relates

to a constant-voltage circuit that is capable of

performing phase compensation using a low ESR

10   (Equivalent Serial Resistance) capacitor by

providing a circuit for compensating for a voltage

drop of an output voltage caused by an output

resistance.

BACKGROUND ART

15   Conventionally, a power unit that is

capable of compensating for a voltage drop at a load

due to wiring without using two remote sensing lines

for low cost has been available, for example, as

disclosed by Patent Reference 1.

20   Further, in order to perform phase

compensation for a constant-voltage circuit,

conventionally, a capacitor is often provided at the

output terminal of the constant-voltage circuit in

parallel to the load as shown in Fig. 3. An internal

25   impedance of ESR and a capacitance of a capacitor

C101 provide the phase compensation, and improve the
frequency characteristics of the constant-voltage
circuit by moving a pole and generating a zero point
in the frequency characteristics. Since the
5   advantage of this method is that the constant-
voltage circuit does not have to provide a terminal
for phase compensation, the number of terminals of a
power supply IC can be small. For such phase
compensation method, a tantalum capacitor having a
10   great ESR is normally used.

As shown in Fig. 4, the typical ESR of a
tantalum capacitor having a capacitance of 2.2 μF
ranges from 1 Ω to 10 Ω, which ESR provides the
zero point at a desirable region in the frequency
15   characteristics of the constant-voltage circuit for
phase compensation, and accordingly, satisfactory
phase compensation is available. Nevertheless,
recently and continuing, ceramic capacitors that are
smaller and lighter-weight than tantalum capacitors,
20   having a large capacitance, are available with a
stable supply at low cost. Accordingly, requirements
for using the ceramic capacitor as the capacitor for
the phase compensation are increasing.

Here, the ESR of the ceramic capacitor is
25   small, ranging from 10 mΩ to 30 mΩ, which is 100 to

1000 times smaller than the tantalum capacitor as shown in Fig. 5. Accordingly, when the ceramic capacitor is used for phase compensation, the frequency at which a zero point is obtained moves to

5 a very high frequency, and suitable phase compensation cannot be obtained.

In order to lower the frequency at which the zero point is obtained, a solution may be to insert a resistor in series with the ceramic

10 capacitor, the resister being provided outside of a power supply IC (constant voltage IC). However, it is disadvantageous for space and cost reasons. Accordingly, it is preferred that the resistor be provided inside the power supply IC.

15 Fig. 6 and Fig. 7 show examples of a circuit where a resistor is provided in the power supply IC.

The example shown in Fig. 6 includes a terminal PinVout2, which is an IC package terminal,

20 for connecting a ceramic capacitor, a fixed resistor R103 having a resistance value of about 100 mΩ for phase compensation provided between a pad ICP2 of the IC chip and the terminal PinVout2, and an output terminal PinVout1 for outputting a voltage. In a

25 case like this, since the output current io does not

flow through the fixed resistor R103, the output

voltage is stably available.

In the case of the example shown in Fig. 7,

the resistance value of the fixed resistor R103 for

5 phase compensation ranges from 100 mΩ to 10 Ω, the

resistor R103 being provided between a pad ICP of

the IC chip and the output terminal PinVout of the

IC.

While in the case of the example shown in

10 Fig. 7, the number of IC terminals is smaller than

the example of Fig. 6, the output current io flows

through the fixed resistor R103. When the output

current io becomes great, a voltage drop Vdrop (=io

x resistance of R103) across the fixed resistor R103

15 cannot be neglected. In order to compensate for the

voltage drop Vdrop, a resistor R104 having a fixed

resistance value is inserted between a reference

voltage source Vref and the grounding voltage, a

load is connected between the output terminal

20 PinVout and the resistor R104, and the same output

current io flows through the fixed resistor R104 and

the load.

According to this arrangement, if the

output current io increases, a voltage drop across

25 the fixed resistor R104 increases, and a voltage of

the non-inverted input terminal of an error

amplifying circuit AMP into which the reference

voltage Vref is input rises. For this reason, an

internal output voltage Vo of the constant-voltage

5   circuit is raised, and the voltage drop Vdrop due to

the fixed resistor R103 is compensated for. In order

to completely remove the influence of the fixed

resistor R103, relations between resistors R101 and

R102 for output voltage detection, and the fixed

10   resistors R103 and R104 are set as

(resistance of R101)/(resistance of R102)

=(resistance of R103)/(resistance of R104).

However, if (resistance of

R101)/(resistance of R102) <(resistance of

15   R103)/(resistance of R104), positive feedback starts

occurring, and the output voltage rises. Accordingly,

the relations are usually made into

(resistance of R101)/(resistance of R102)

>=(resistance of R103)/(resistance of R104).

20   [Patent reference 1] JPA 10-257764

[Description of the Invention]

[Problem(s) to be solved by the Invention]

As described above, the example shown in

Fig. 6 has a problem in that an additional IC

25   terminal is required as compared with the example

shown in Fig. 7, which problem becomes real when an IC has a limit to the number of terminals. As for the example shown in Fig. 7, since the fixed resistor R104 is inserted between the load and the

5　grounding voltage, the low end voltage of the load, which is connected to the resistor R104, is not equal to the ground voltage, which poses a problem when transmitting/receiving a signal to/from a load that is connected to another power supply.

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DISCLOSURE OF THE INVENTION

Accordingly, an object of the present invention is to solve the problems and to offer a constant-voltage circuit that is capable of

15　providing a constant voltage that does not cause a problem in transmitting/receiving a signal to/from a load connected to another power supply. In summary, according to the present invention, a current that is proportional to an output current is provided to

20　a part of resistances for output voltage detection, which raises an internal output voltage of the constant-voltage circuit. In this manner, while a voltage drop through a resistance for phase compensation is compensated for, a small capacitor

25　having a small ESR, like a ceramic capacitor, can be

used for phase compensation. Further, the low side voltage of the load is made to be equal to the grounding voltage.

[Means for Solving the Problem]

5   The constant-voltage circuit of the present invention for converting an input voltage provided to an input terminal of the constant-voltage circuit into a predetermined constant voltage, and for providing the constant voltage to a

10   load includes:

a reference voltage generating circuit unit for generating and outputting a predetermined reference voltage;

an output voltage detecting unit for

15   detecting the constant voltage, and generating and outputting a voltage that is proportional to the detected voltage;

an output transistor for outputting a current provided from the input terminal to the load

20   according to a control signal;

an error amplifying circuit unit for providing the control signal for controlling operations of the output transistor so that the proportional voltage become equal to the reference

25   voltage;

an output current detecting unit for
detecting the current output from the output
transistor, and generating and outputting the
proportional current that is proportional to the
5   detected current;

a first resistance connected to the output
voltage detecting unit;

a proportional current supply circuit unit
for supplying the proportional current that is
10   proportional to the output current from the output
current detecting unit to the first resistance;

a second resistance connected between the
output transistor and the load; and

a capacitor connected to a junction where
15   the second resistance and the load are connected,
wherein the second resistance and the capacitor
constitute a phase compensating circuit unit for
carrying out phase compensation of the error
amplifying circuit unit.

20   According to the constant-voltage circuit
of the present invention, a resistance value of the
first resistance is set such that a product of the
resistance value and the proportional current
provided by the output current detecting unit become
25   equal to or less than a voltage drop across the

second resistance.

The constant-voltage circuit is arranged such that the output current detecting unit includes a transistor for output current detection for outputting the current from the input terminal that is in proportion to a value of the current output from the output transistor according to the control signal from the error amplifying circuit unit.

The constant-voltage circuit is arranged such that the proportional current supply circuit unit includes a current mirror circuit, to which the current output from the transistor for output current detection is provided.

According to an aspect of the present invention, the proportional current supply circuit unit of the constant-voltage circuit includes a stack type current mirror circuit.

According to an aspect of the present invention, the proportional current supply circuit unit of the constant-voltage circuit includes two current mirror circuits that are cascoded.

According to an aspect of the present invention, the proportional current supply circuit unit of the constant-voltage circuit includes a Wilson type current mirror circuit.

According to an aspect of the present invention, the proportional current supply circuit unit includes:

an operation amplifying circuit, wherein

5   the output of the output transistor is provided to one of input terminals of the operation amplifying circuit, and the output of the transistor for output current detection is provided to another input terminal of the operation amplifying circuit;

10   a current control transistor for controlling the current output from the transistor for output current detection according to an output of the operation amplifying circuit, and for outputting a control current; and

15   a current mirror circuit that inputs the control current output by the current control transistor, and for outputting a current proportional to the control current to the first resistance.

20   According to an aspect of the present invention, the capacitor of the constant-voltage circuit is small, and a ceramic capacitor, for example, is used.

According to an aspect of the present

25   invention, a resistance value of the second

resistance in the constant-voltage circuit is set between 50 mΩ and 10 Ω.

According to an aspect of the present invention, the second resistance of the constant-voltage circuit is formed by wiring resistance.

According to an aspect of the present invention, the reference voltage generating circuit unit, the output voltage detecting unit, the output transistor, the error amplifying circuit unit, the output current detecting unit, the first resistance, and the proportional current supply circuit unit are integrated as an IC.

According to an aspect of the present invention, the reference voltage generating circuit unit, the output voltage detecting unit, the output transistor, the error amplifying circuit unit, the output current detecting unit, the first resistance, the proportional current supply circuit unit, and the second resistance are integrated as an IC.

According to an aspect of the present invention, the first resistance of the constant-voltage circuit may be connected between the output transistor and the output voltage detecting unit.

[Effect of the Invention]

As described above, according to the

constant-voltage circuit of the present invention,

the internal output voltage of the constant-voltage

circuit is raised by a current proportional to the

output current to a part of output voltage detection

5   resistances. In this manner, the voltage drop by the

resistance prepared for phase compensation is

compensated for, and a capacitor having a small

internal resistance like a ceramic capacitor can be

used for phase compensation. Further, the low side

10   voltage of the load is made equal to the grounding

voltage, providing stable signal transfer to and

from the load.

BRIEF DESCRIPTION OF THE DRAWINGS

15   Fig. 1 is an example circuit diagram of a

constant-voltage circuit according to a first

embodiment of the present invention.

          Fig. 2 is another example circuit diagram

of the constant-voltage circuit according to the

20   first embodiment of the present invention.

          Fig. 3 is an example circuit diagram of a

conventional constant-voltage circuit.

          Fig. 4 shows an example of an equivalent

circuit of a tantalum capacitor.

25   Fig. 5 shows an example of an equivalent

circuit of a ceramic capacitor.

Fig. 6 is an example circuit diagram of a
conventional constant-voltage circuit.

Fig. 7 is an example circuit diagram of

5   another conventional constant-voltage circuit.

BEST MODE FOR CARRYING OUT THE INVENTION

In the following, embodiments of the
present invention are described with reference to

10 the accompanying drawings.

[First Embodiment]

Fig. 1 shows an example of a circuit of a
constant-voltage circuit 1 according to the first
embodiment of the present invention.

15   The constant-voltage circuit 1 includes a
constant-voltage circuit unit 2 and a phase
compensating circuit unit 3. The constant-voltage
circuit unit 2 is for generating a predetermined
constant voltage from a supply voltage Vdd, and

20 outputs the constant voltage as an internal output
voltage Vo. The phase compensating circuit unit 3
includes a resistor R3 and a capacitor C1, and
performs phase compensation to the constant-voltage
circuit unit 2.

25   The constant-voltage circuit unit 2

further includes an error amplifying circuit AMP1, a

reference voltage generating circuit 11 for

generating and outputting a predetermined reference

voltage Vref that is provided to a non-inverted

5   input terminal of the error amplifying circuit AMP1,

an output transistor M1 that is a PMOS transistor

for controlling an output current io that is

provided to the phase compensating circuit unit 3

according to a signal output from the error

10   amplifying circuit AMP1, and resistors R1, R2, and

R4 for detecting the internal output voltage Vo.

Further, the constant-voltage circuit unit 2

includes a transistor M2 that is a PMOS transistor

for detecting the output current io, and a current

15   mirror circuit 12. The current mirror circuit 12

includes PMOS transistors M3 and M4, and NMOS

transistors M5 and M6.

In addition, the reference voltage

generating circuit 11 serves as the reference

20   voltage generating circuit unit, the error

amplifying circuit AMP1 serves as an error

amplifying circuit unit, and the resistors R1 and R2

serve as an output voltage detecting unit. Further,

the transistor M2 serves as an output current

25   detecting unit, the resistor R4 serves as a first

resistance, the current mirror circuit 12 serves as a proportional current supply circuit unit, and the resistor R3 serves as a second resistance.

5   The inverted input terminal of the error amplifying circuit AMP1 is connected to a connection point where the resistors R1 and R2 are connected, and the output terminal of the AMP1 is connected to the gate of the output transistor M1. The output transistor M1 is connected between the supply

10   voltage Vdd, which is an input voltage, and an output pad 15, called an IC pad 15, of the IC, the IC pad 15 being the output terminal of the constant-voltage circuit unit 2. The resistors R4, R1, and R2 are connected in series between the drain of the

15   output transistor M1, and the grounding voltage. The gate of the output transistor M1 is connected to the output terminal of the error amplifying circuit AMP1. As for the transistor M2 for output current detection, the source is connected to the supply

20   voltage Vdd.

Between the drain of the transistor M2 for output current detection, and the grounding voltage, the PMOS transistor M4 and the NMOS transistor M6 are connected in series, and the PMOS transistor M3

25   and the NMOS transistor M5 are connected in series

between the connection point of the resistors R4 and

R1, and the grounding voltage. The gate of the PMOS

transistor M3 and the gate of the PMOS transistor M4

are connected, and the connection point thereof is

5   connected to the drain of the PMOS transistor M3.

Further, the gate of the NMOS transistor M5 and the

gate of the NMOS transistor M6 are connected, and

the connection point thereof is connected to the

drain of the NMOS transistor M6.

10   In the configuration as described above,

the error amplifying circuit AMP1 controls the gate

voltage of the output transistor M1 so that the

voltages of the input terminals of the error

amplifying circuit AMP1 become equal to each other.

15   Accordingly, the internal output voltage Vo of the

constant-voltage circuit unit 2 when the output

current io is zero is expressed by the following

formula (1). Here in the formula (1), R1, R2, and R4

represent resistance values of the resistors R1, R2,

20   and R4, respectively.

$$Vo = Vref \times (R4+R1+R2)/R2 \dots \dots (1)$$

The internal output voltage Vo is provided

from the output terminal Pout of the IC through the

IC pad 15 and the fixed resistor R3 for phase

25   compensation. Between the output terminal Pout of

the IC and the grounding voltage, a load 10 is connected with a capacitor C1 for phase compensation in parallel.

Since the fixed resistor R3 for phase

5   compensation is provided in the IC, a ceramic capacitor having a small ESR can serve as the capacitor C1.

However, as the output current io increases, a voltage drop Vdrop increases across the

10   fixed resistor R3 for phase compensation, and the voltage Vout of the output terminal Pout is decreased accordingly. The transistor M2 for output current detection, the current mirror circuit 12, and the resistor R4 constitute a circuit for

15   compensating for the voltage drop Vdrop.

The gates of the transistor M2 and the transistor M1 are connected, and the sources of the transistor M2 and the transistor M1 are connected, constituting a current mirror circuit. The drain

20   current of the transistor M2 is set at, e.g., between 1/10000 and 1/1000 of the drain current of the transistor M1.

The drain current of the transistor M2 is provided to the current mirror circuit 12, the

25   channel length modulation effect of which is

improved. Although the current mirror circuit 12
shown in Fig. 1 is constituted by a stack type
circuit, a cascading current supply, a Wilson type
current mirror circuit, and the like may be used.

5   An output current i3 of the current mirror
circuit 12 is taken out as the source current of the
PMOS transistor M3. If the mirror current ratio of
the current mirror circuit 12 is set at 1:1, the
source current i3 of the PMOS transistor M3 becomes

10   equal to the drain current of the transistor M2 for
output current detection. (Note: Output current i3
is output as viewed from transistor M1, but input as
viewed by transistor M3. This is okay as
translated.)

15   Since the source of the PMOS transistor M3
is connected to the connection point of the resistor
R4 and the resistor R1, the source current i3 of the
PMOS transistor M3 flows through the resistor R4,
and a voltage drop equal to the resistance of R4 x

20   i3 is generated across the resistor R4. (Note: You
are correct that i2 = i3 + i1, but i3 is the part
that is changing. The translation is good)

          Consequently, since the voltage drop
across the resistor R4 increases as the output

25   current io increases, the internal output voltage Vo

of the constant-voltage circuit unit 2 is raised, and the voltage drop Vdrop generated by the resistor R3 for phase compensation can be compensated for.

This situation is further explained using
5   the following formulas. Here, in each formula, R1 through R4 represent resistance values of the resistors R1 through R4, respectively.

The internal output voltage Vo of the constant-voltage circuit unit 2 is expressed by the
10   following formula (2).

$$Vo = Vref \times (R4+R1+R2)/R2 + R4 \times i3 \ .. \ (2)$$

Further, the voltage Vout of the output terminal Pout is expressed by the following formula (3).

15   $$Vout = Vo-R3 \times io \ .... \ (3)$$

By substituting the formula (2) into the formula (3), the following formula (4) is obtained.

$$Vout = Vref \times (R4+R1+R2)/R2 + R4 \times i3$$
$$-R3 \times io \ .... \ (4)$$

20   In reference to the formula (4), a condition that makes $R4 \times i3-R3 \times io = 0$ provides an ideal voltage compensation.

Accordingly, the condition is $R4 \times i3 = R3 \times io$.

Provided that $io/i3 = A$ (A is a constant),
25   the condition is that $R4 = A \times R3$. That is, the

condition is that the resistance of the resistor R4 be A times of the resistance of the resistor R3. However, if R4xi3 becomes greater than R3xio, positive feedback starts. Accordingly, the value of

5 the constant A is usually set equal to or smaller than io/i3.

Fig. 2 shows another example circuit of a constant-voltage circuit 1a according to the first embodiment of the present invention. Here in Fig. 2,

10 the components the same as in Fig. 1 are given the same reference marks, and explanations thereof are not repeated, but differences are described in the following.

The differences include that the current

15 mirror circuit 12 of Fig. 1 is replaced by a current mirror circuit 12a. The PMOS transistor M3 of the current mirror circuit 12 is not used in the current mirror circuit 12a, wherein an operation amplifying circuit AMP2 is added, and the transistors M5 and M6

20 constitute a single-stage current mirror circuit. In this connection, the constant-voltage circuit unit is referred to as the constant-voltage circuit unit 2a, and the constant-voltage circuit is referred to as the constant-voltage circuit 1a in Fig. 2.

25 With reference to Fig. 2, the constant-

voltage circuit 1a includes the constant-voltage circuit unit 2a and the phase compensating circuit unit 3. The constant-voltage circuit unit 2a is for generating a predetermined constant voltage from the

5   supply voltage Vdd, which is an input voltage, and outputs the constant voltage as the internal output voltage Vo. The phase compensating circuit unit 3 performs phase compensation for the internal output voltage Vo output from the constant-voltage circuit

10   unit 2a, and supplies the phase-compensated voltage to the load 10.

The constant-voltage circuit unit 2a includes the reference voltage generating circuit 11, the error amplifying circuit AMP1, the output

15   transistor M1, the resistors R1, R2, and R4 for output voltage detection, the transistor M2 for output current detection, and the current mirror circuit 12a. The current mirror circuit 12a includes the operation amplifying circuit AMP2, the PMOS

20   transistor M4, and the NMOS transistors M5 and M6. In addition, current mirror circuit 12a serves as the proportional current supply circuit unit, and the PMOS transistor M4 serves as a current control transistor.

25   Between the drain of the transistor M2 for

output current detection, and the grounding voltage,

the PMOS transistor M4 and the NMOS transistor M6

are connected in series, and the NMOS transistor M5

is connected between the connection point of the

5   resistors R4 and R1, and the grounding voltage. The

gate of the PMOS transistor M4 is connected to the

output terminal of the operation amplifying circuit

AMP2, the internal output voltage Vo is provided to

the non-inverted input terminal of the operation

10   amplifying circuit AMP2, and the source of the PMOS

transistor M4 is connected to the inverted input

terminal of the operation amplifying circuit AMP2.

Further, the gate of the NMOS transistor M5 and the

gate of the NMOS transistor M6 are connected, and

15   the connection point is connected to the drain of

the NMOS transistor M6.

      In a such configuration, the drain current

of the PMOS transistor M4 serves as the input

current for the current mirror circuit constituted

20   by the NMOS transistors M5 and M6, and the current

mirror circuit provides the drain current of the

NMOS transistor M5 to the resistor R4. (Note: Yes,

the wording is strange but the arrow is correct.)

      In this way, the current mirror circuit

25   constituted by the NMOS transistors M5 and M6 is

inserted in the feedback loop of the operation

amplifying circuit AMP2. Accordingly, the current

mirror circuit 12a controls the gate voltage of the

PMOS transistor M4 so that the drain voltage of the

5   output transistor M1 and the drain voltage of the

transistor M2 for output current detection are made

equal. For this reason, precision of the current of

the current mirror circuit 12 can be further raised

as compared with the case shown by Fig. 1.

10   As described above, the constant-voltage

circuit according to the first embodiment of the

present invention is capable of compensating for not

only the voltage drop across the resistor R3 for

phase compensation connected to the IC pad 15, but

15 also a gain fall of the error amplifying circuit

AMP1, and a voltage drop by a wiring resistance from

the constant-voltage circuit unit 2 to the load 10.

          Further, the present invention is not

limited to these embodiments, but various variations

20 and modifications may be made without departing from

the scope of the present invention.